What Is Claimed Is:

1. A die comprising:

an integrated circuit;

a first scribe seal around said integrated circuit; and

a second scribe seal around said first scribe seal, wherein all of said integrated circuit, said first scribe and said second scribe seal are laid on a common substrate.

2. The die of Claim 1, wherein said first scribe seal comprises a first plurality of layers, and said second scribe seal comprises a second plurality of layers, wherein said first plurality of layers are laid differently than said second plurality of layers on said die.

3. The die of Claim 1, wherein said first scribe seal prevents entry of mobile ions into said integrated circuit, said second scribe seal provides mechanical strength to said die, and both of said first scribe seal and said second scribe seal provide respective high resistance paths along said common substrate.

4. The die of Claim 3, wherein said first scribe seal comprises:

a thin metal layer to provide high resistance path; and

a metal layer and a via layer together forming a wall in an oxide layer, wherein said wall prevents the entry of said mobile ions into said integrated circuit.

5. The die of Claim 4, wherein said second scribe seal comprises a thick metal layer providing mechanical strength to said die, wherein said thick metal layer is not connected to said common substrate to provide high resistance path to said common substrate.

6. The die of Claim 5, wherein a diffusion layer is absent in said second scribe seal.

7. The die of Claim 6, wherein a contact layer is absent in said second scribe seal.

8. The die of Claim 5, wherein said integrated circuit comprises an analog portion and a digital portion.

9. The die of Claim 1, further comprising a gap separating said first scribe seal from said second scribe seal.

10. A method of manufacturing a die, said method comprising:

(a) laying a first scribe seal around an integrated circuit on a common substrate; and

(b) laying a second scribe seal around said first scribe seal on said common substrate.

11. The method of Claim 10, wherein said (a) comprises laying a first plurality of layers, and said (b) comprises laying a second plurality of layers, wherein said first plurality of layers are laid differently than said second plurality of layers on said die.

12. The method of Claim 10, wherein said (a) prevents entry of mobile ions into said integrated circuit, said (b) provides mechanical strength to said die, and both of said first scribe seal and said second scribe seal provide respective high resistance paths along said common substrate.

13. The method of Claim 12, wherein (a) comprises:

laying a thin metal layer to provide high resistance path; and

laying a metal layer and a via layer, which together form a continuous path through an oxide layer.

14. The method of Claim 13, wherein said (a) comprises laying a thick metal layer providing mechanical strength to said die, wherein said thick metal layer is not connected to said common substrate to provide high resistance path to said common substrate.

15. The method of Claim 14, wherein a diffusion layer is not laid in said (b) in a portion corresponding to said second scribe seal.

16. The method of Claim 15, wherein a contact layer is not laid in said (b) in a portion corresponding to said second scribe seal.

17. The die of Claim 14, wherein said integrated circuit comprises an analog portion and a digital portion.

18. The method of Claim 10, further comprising providing a gap between said first scribe seal and said second scribe seal.